REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendments and the following remarks.

The Applicants originally submitted Claims 1-20 in the application. While Claims 1, 2, 5, 7-9, 12, 14-16 and 20 have been rejected, Claims 3, 4, 10, 11, 13, and 17-19 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Claims 1-20 are currently pending in the application.

I. Specification

The Examiner has objected to the title of the invention for not being descriptive. In accordance with the Examiner's suggestion, the Applicants have amended the title of the invention to overcome the objection thereto.

II. Rejection of Claims under 35 U.S.C. §102

The Examiner has rejected Claims 1, 2, 7-9, 14-16 and 20 under 35 U.S.C. §102(a) as being anticipated by U.S. Patent No. 6,791,305 to Imai, *et al.* ("Imai"). As the Examiner is no doubt aware, anticipation requires that each and every element of the claimed invention be

disclosed in a single prior art reference; the disclosed elements must either be disclosed expressly or inherently and must be arranged as in the rejected claims.

The Examiner asserts that Imai discloses the controller, method and power converter of Claims 1, 8 and 15, respectively. More specifically, the Examiner believes that Imai discloses an oscillator configured to provide a clock signal having multiple phases (multiple phases CLK1-CLK3, *e.g.*, column 4, lines 54-58). According to the Examiner, Imai also discloses a modulator configured to select a phase of the clock signal as a function of a portion of a digital duty cycle signal (column 4, lines 46-54) to refine a resolution of the duty cycle and provide a signal to control the duty cycle of a switch as a function of the digital duty cycle signal. (Examiner's Action, page 3). The Applicants respectfully disagree.

As illustrated in FIGURE 1, Imai discloses a switching power supply having a switching circuit block 10, an output circuit block 20 and a control circuit block 30. The control circuit block 30 is a digital control circuit consisting of an analog-to-digital (A/D) converter 31, reference voltage generating circuit 32, subtracter 33, latch circuit 34 and arithmetic circuit 35. The A/D converter 31 is a circuit that receives an output voltage V_o appearing at an output power terminal 3 and converts this to a digital value in response to a clock signal CLK1. The digital value which is the output of the A/D converter 31 is called an "output voltage digital value D1." The reference voltage generating circuit 32 is a circuit that generates a digital value corresponding to the target value of the output voltage V_o; the output value of the reference voltage generating circuit 32 is called a "reference voltage digital value D2." The subtracter 33 is a logic circuit (logic gate circuit) that subtracts the reference voltage digital value D2 from output voltage digital value D1 to derive an "error voltage digital value D3." The latch circuit 34 is a multi-bit latch circuit that latches the error voltage digital value in response to the clock signal

CLK3; this output is called the "control digital value D4." (Column 3, line 56 to column 4, line 10.)

The arithmetic circuit 35 is a circuit that receives the control digital value D4 supplied from latch circuit 34 and controls the switching operations of switch elements 12, 13 of the switching circuit block 10 based thereupon. Specifically, the greater the control digital value D4 is in the positive direction, namely the greater the output voltage digital value D1 is in excess of the reference voltage digital value D2, the duty of switch element 12 is controlled to be smaller (the duty of switch element 13 is controlled to be larger). Conversely, the greater the control digital value D4 is in the negative direction, namely the greater the reference voltage digital value D2 is in excess of the output voltage digital value D1, the duty of switch element 12 is controlled to be larger (the duty of switch element 13 is controlled to be smaller). Thereby, the actual output voltage V_o is stabilized to the value indicated by the reference voltage digital value D2. (Column 4, lines 11-26.)

A reference voltage generating circuit 32 of Imai is illustrated and described with respect to FIGURE 2 thereof. The reference voltage generating circuit 32 consists of a plurality of memories 40-1, 40-n and a multiplexer 41. The memories 40-1, 40-n each contain a digital value (target digital value) corresponding to a different output voltage V_o. Here, a different output voltage V_o refers to the various operating voltages when a DC load 5 demands variable operating voltages. For example, if the DC load 5 demands three different operating voltages of 1.0 V, 1.3 V and 1.5 V, then target digital values corresponding to 1.0 V, 1.3 V and 1.5 V are stored in memories 40-1, 40-3, respectively. Note that the target digital values are set to the same values as the output voltage digital value D1 to be obtained from the A/D converter 31 in the case that the actual output voltage V_o agrees with the target value. The target digital values V_{ref1}, V_{refn}

stored in the memories 40-1, 40-n are each supplied to the multiplexer 41. (Column 4, lines 28-45.)

The multiplexer 41 is a circuit that receives the target digital values V_{ref1}, V_{refm}, the clock signal CLK2 and the selection signal SEL and, synchronized to the clock signal CLK2, supplies the target digital value (one of V_{ref1} through V_{refn}) indicated by the selection signal SEL to the subtracter 33 as the reference voltage digital value D2. The selection signal SEL is a signal given by the DC load 5 to specify the output voltage V_o to be supplied. The clock signals CLK1, CLK2, and CLK3 preferably agree with each other in frequency, and the phases of at least clock signals CLK1 and CLK3 and the phases of clock signals CLK2 and CLK3 are essentially shifted. (Column 4, lines 46-58.)

The Examiner relies on the previous statement as a teaching that Imai discloses a modulator configured to select a phase of the clock signal as a function of a portion of a digital duty cycle signal to refine a resolution of the duty cycle and provide a signal to control the duty cycle of a switch as a function of the digital duty cycle signal. Again, the Applicants respectfully disagree.

Regarding the present application, FIGURE 5 illustrates a block diagram of portions of a controller including an embodiment of a modulator constructed according to the principles of the present invention. In the illustrated embodiment, an implementation of an exemplary gate modulator is provided using a four bit digital word representing a digital duty cycle signal S_D provided by a controller (see, for instance, the controller 120 illustrated and described with respect to FIGURE 1). For the purposes of an example, the digital word "1001" corresponds to the fourth through the first bits S_{D3}, S_{D2}, S_{D1}, S_{D0}, respectively, of the digital duty cycle signal S_D. An illustrative two-stage oscillator coupled to the modulator provides multiple phases of a clock

signal (such as the clock signal $S_{CLK-OSC}$ illustrated and described with respect to FIGURE 1), namely, first, second, third and fourth phases $ph_0,\ldots, ph_3$. (Page 20, paragraph 52.)

A portion (*e.g.*, two bits) of the digital word is employed to select one of the four oscillator phases from the oscillator and represents the least significant bits (also referred to as "LSBs") of the digital word. In the example, the least significant bits are "01," which correspond to the second and first bits S_{D1}, S_{D0}, respectively, of the digital duty cycle signal S_D. The remaining two bits ("10," which correspond to the fourth and third bits S_{D3}, S_{D2}, respectively, of the digital duty cycle signal S_D) represent the most significant bits (also referred to as "MSBs") of the digital word. Of course, the number of bits forming the digital word of the digital duty cycle signal S_D may be different in conjunction with the number of phases of the oscillator and still be within the broad scope of the present invention. (Page 20, paragraph 53.)

The modulator includes a multiplexer MUX and the first, second, third and fourth phases $ph_0,\ldots, ph_3$ from the oscillator are supplied thereto. In the illustrated embodiment, the multiplexer MUX is a four-to-one multiplexer that is controlled by the least significant bits (first and second bits S_{D0}, S_{D1} of the digital duty cycle signal S_D). The multiplexer MUX provides a multiplexer output signal PHASE_LSB corresponding to the one of the phases $ph_0,\ldots,ph_3$ selected in accordance with the first and second bits S_{D0}, S_{D1} of the digital duty cycle signal S_D. For the purposes of the present example, the multiplexer MUX selected the second phase ph_1 in accordance with first and second bits S_{D0}, S_{D1} of the digital duty cycle signal S_D. The multiplexer output signal PHASE_LSB is coupled to a clock input CK of a first flip-flop (*e.g.*, a D flip-flop) D_1. (Page 21, paragraph 54.)

The modulator disclosed in the present application provides time resolution for an exemplary four-bit signal representing a duty cycle with one-sixteenth precision when the frequency of the oscillator is only four times higher than the switching frequency of the power converter. The additional factor of four in resolution is obtained in the implementation described above by selectively coupling one of the four phases $ph_0,\ldots,ph_3$ of an oscillator to an input of a first flip-flip D_1. A pulse width modulated signal S_{PWM} is therefore produced in combination with the most significant bits of the digital duty cycle signal S_D provided to a counter CTR and the least significant bits of the digital duty cycle signal S_D provided to the multiplexer MUX. By employing selected phases $ph_0,\ldots,ph_3$ of an oscillator under the control of the least significant bits of the digital duty cycle signal S_D, the modulator can be configured to provide time resolution substantially finer than a frequency of an oscillator. (Page 23, paragraph 58.)

In contrast to Imai, therefore, the inventions as recited in Claims 1, 8 and 15 select a phase of a clock signal as a function of a portion of a digital duty cycle signal to refine a resolution of a duty cycle of a switch. While Imai employs a phase shift in clock signals, the reference fails to select a phase of a clock signal as a function of a portion of a digital duty cycle signal. With regard to Imai and as illustrated in FIGURE 3 thereof, the phase shift of the clock signal CLK3 with respect to clock signals CLK1 and CLK2 is selected to be larger than the longer of the time delays T1 or T2 plus time delay T3, regardless of the timing on which the selection signal SEL supplied from a DC load 5 changes. The latch circuit 34 will not perform its latch during an indefinite period of the error voltage digital value D3, and a smooth switching of the output voltage V_o can be achieved. To wit, it is possible to achieve high-precision and high-speed switching of the output voltage V_o without disturbance of the output voltage V_o by the order to switch the output voltage V_o. (Column 5, lines 42-45.) Thus, the phase shift

disclosed in Imai is not only employed for a different purpose, but Imai fails to select a phase of a clock signal as a function of a portion of a digital duty cycle signal to refine a resolution of a duty cycle of a switch as recited in Claims 1, 8 and 15 of the present application. To reiterate, the phase shift mentioned in Imai is a pre-selected value to accommodate the delays as described above whereas the selection of the clock signal of the claimed invention is an adaptive selection as a function of a portion of the digital duty cycle.

Thus, Imai does not disclose each and every element of Claims 1, 8 and 15, and the claims dependent thereon, and, as such, is not an anticipating reference. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection in view of Imai with respect to Claims 1, 2, 7-9, 14-16 and 20.

III. Rejection of Claims under 35 U.S.C. §103

The Examiner has rejected Claims 5, 12 and 18 under 35 U.S.C. §103(a) as being unpatentable over Imai, as applied above, and further in view of U.S. Patent No. 5,689,213 to Sher. The Examiner asserts that Imai teaches the invention as described above but fails to specifically recite a ring oscillator as a means for creating a clock signal. Sher, however, discloses a ring oscillator to create clock signals as illustrated in FIGUREs 4A to 4C. According to the Examiner, it would have been obvious at the time of the invention to use the ring oscillator of Sher in combination with Imai because a ring oscillator can be programmed after manufacture to attain greater accuracy (*e.g.*, Sher, column 3, lines 15-34). (Examiner's Action, pages 4-5). The Applicants respectfully assert that the claimed invention is not obvious in view of the

foregoing references, and that the Examiner has failed to establish a *prima facie* case of obviousness of the aforementioned claims.

For the reasons as set forth above, Imai fails to teach or suggest selecting a phase of a clock signal as a function of a portion of a digital duty cycle signal to refine a resolution of a duty cycle of a switch in accordance with the controller, related method and power converter as recited in Claims 1, 8 and 15. Imai, therefore, fails to teach or suggest all of the elements of Claims 1, 8 and 15, and Sher, by the Examiner's own admission, does not even address such a structure or methodology. Thus, since Imai fails to teach or suggest all of the elements of Claims 1, 8 and 15, and Sher fails to cure the deficiencies thereof, the Examiner cannot establish a *prima facie* case of obviousness of Claims 5, 12 and 18, which respectively depend therefrom.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 5, 12 and 18 under 35 U.S.C. §103(a). In accordance therewith, the Applicants respectfully request the Examiner withdraw the rejection.

IV. Conclusion

In view of the foregoing amendments and remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-20.

The Applicants request that the Examiner telephone the undersigned attorney of record at (972) 732-1001 if such would further expedite the prosecution of the present application. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

August 25, 2005
Date

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